Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 29 with the following amended paragraph:

Figure 1 illustrates peer-to-peer connections according to the IEEE 1394 standard. A computer 102 in a room 104 of a structure 100 is communicatively coupled to a computer 106 in a room 108 of the structure 100 via a serial bus 105. Another serial bus 109 is used to communicatively couple the computer 106 to another computer 110 in another room 112. Each computer on the network includes networking components that implement IEEE 1394.

Please replace the paragraph beginning on page 2, line 4 with the following amended paragraph:

Figure 2 illustrates the IEEE 1394 networking components 200 that include a physical layer chip ("PHY") 202 and a link layer chip ("LINK") 204. The LINK chip 204 contains the networking intelligence to process and generate networking signals, such as arbitration signals and packets. The PHY chip 202 is the physical interface by which the computer system may receive or send networking information to and from the serial bus along a plurality of signal lines 218_1-218_{14}. The PHY chip 202 also serializes the data from the LINK chip 204 if the data is to be sent out to the serial bus 220, and likewise deserializes the data from the cable to be sent to the LINK chip 204 in parallel format. There are typically at least fourteen wires that communicatively couple the PHY chip 202 to the LINK chip 204.

Please replace the paragraphs beginning on page 7, line 11 and continuing through to page 8, line 29 with the following amended paragraphs:

Figure 4 illustrates a cross sectional view of another package assembly 400 according to another embodiment of the present invention where first and second integrated circuits 416, 418 are incorporated within a single module 404 while remaining electrically isolated. Methods and materials for manufacturing a single module having two or more semiconductors are well-known in the art, and will not be described in detail herein. A capacitor is formed by the ground pin (not shown) of the first integrated circuit 416 that is conductively coupled to the first conductive surface 410, which is positioned adjacent to a substrate 402.

[spaced apart from the] The second integrated circuit 418 is conductively coupled by its ground pin (not shown) to the second conductive surface 412 using wires 406 or any other suitable conductive coupling. A dielectric is interposed between the first conductive layer 4110 and the second conductive layer 412. As in the previous embodiment, a resistor 408 may be coupled to the first conductive layer 410 and the second conductive layer 412 to permit electrical potential equilibration when the package is de-energized.

Figure 5 illustrates another package assembly 500 according to still another embodiment of the present invention where the package assembly has electronic modules 504, 505 on separate substrates 502, 503 within the assembly. In this embodiment, a first electronic module 504 is attached to a first substrate 502 and a second electronic module 505 attached to a second substrate 503 are spaced apart by the first and second conductive surfaces 510, 512 and the dielectric 514. As with other embodiments of the invention, the first and second electronic modules 504, 505 are conductively coupled to the first and second conductive surfaces 510, 512 respectively with wire bonds 506 or any other suitable conductive couplings. A dielectric 514 is interposed between the conductive surfaces 510, 512 to prevent direct current from flowing between the conductive surfaces. A resistor 508 may be coupled to the first conductive layer 510 and the second conductive layer 512 to permit electrical potential equilibration when the package is de-energized.

Figure 6 illustrates a package assembly 600 according to yet another embodiment of the present invention, where the capacitor formed by the first and second conductive surfaces 610, 612 and a first dielectric 614 is on the same side of the substrate 602 as the first and second electronic modules 604, 605. The first electronic module 604 and the second electronic module 605 are separated from the second conductive layer 612 by a second dielectric layer 620. The electronic modules 604 and 605 may also be combined into a single structure as shown in Figure 4. Electrical wires 606 couple the first and second modules 604 and 605 to respective first and second conductive layers 610 and 612. A resistor 608 may be coupled to the first conductive layer 610 and the second conductive layer 612 to permit electrical potential equilibration when the package is de-energized.

Figure 7 illustrates a package assembly 700 according to still yet another embodiment of the invention where the first and second electronic modules 704, 705 are stacked

on the substrate 702, as opposed to both being attached to the substrate as illustrated in, for example, Figures 3 and 6. The electronic modules 704, 705 are attached with adhesive at the bondline 718. A first conductive layer 710 is separated from a second conductive layer 712 by a dielectric 714. Electrical wires 706 couple the first and second modules 704 and 705 to respective first and second conductive layers 710 and 712. A resistor 708 may be coupled to the first conductive layer 710 and the second conductive layer 712 to permit electrical potential equilibration when the package is de-energized. Methods and materials for attaching electronic modules with adhesives are well-known in the art, and the details will not be described in detail herein.